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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of	Confirmation No.: 2994
WESTCOTT	Atty. Ref.: 540-508
Serial No. 10/500,623	Group: 2836
Filed: July 2, 2004	Examiner: C. Amaya

For: A SWITCHING CIRCUIT AND A METHOD OF OPERATION THEREOF

* *

APPEAL BRIEF

On Appeal From Group Art Unit 2836

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WESTCOTT — Atty. Ref.: 540-508

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For: A SWITCHING CIRCUIT AND A METHOD OF OPERATION THEREOF

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Commissioner for Patents
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Alexandria, VA 22313-1450

APPEAL BRIEF

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Sir:

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified appeal is BAE SYSTEMS plc by virtue of an assignment of rights from the inventor to BAE SYSTEMS plc recorded July 2, 2004 at Reel 16064, Frame 817.

II. RELATED APPEALS AND INTERFERENCES

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There are believed to be no related appeals, interferences or judicial proceedings with respect to the present application.

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III. STATUS OF CLAIMS

Claims 2-5, 7, 8, 12 and 35-37 have been cancelled without prejudice. Remaining claims 1, 6, 9-11 stand rejected as obvious under 35 USC §103 and claims 13-20 and 23-34 stand rejected under a non-statutory obviousness-type double patenting rejection (there is no specific rejection of claim 40 although it is discussed along with claim 13 in the obviousness double patenting rejection). While the Office Action Summary Sheet indicates that all pending claims are rejected, the text of the Final Rejection identifies no statutory basis for pending claims 21, 22 and 38-42 and thus, they are apparently allowable (except for the indefinite rejection of claim 40 noted above). The Final rejections of claims 1, 6, 9-11, 13-34 and 38-42 (to the extent that claims 21, 22 and 38-42 are actually rejected) are appealed.

IV. STATUS OF AMENDMENTS

No further response has been submitted with respect to the Final Official Action in this application.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Appellant's specification and figures provide an explanation of the claimed invention set out in independent claims 1, 13, 27 and 40, with each claimed

structure and/or method step addressed as to its location in the specification and in the figures.

"1. A pulse width modulation switching circuit, responsive to a voltage demand signal [voltage demand signal 12 shown in Figure 2 and discussed on page 11, lines 10-24 and elsewhere in the specification] , for controlling current supplied to an inductor [electromagnet 10 as shown generally in Figure 2 and discussed on page 11, lines 10-24 and elsewhere in the specification] from a direct current (DC) supply voltage [DC supply 36 as shown in Figure 2 and discussed on page 13, lines 12-27 and elsewhere in the specification], said switching circuit comprising:

a bridge circuit [half-bridge circuit 14 as shown generally in Figure 1 and discussed on page 11, lines 10-24 and elsewhere in the specification], said bridge circuit comprising:

an input operable to receive a direct current, DC, supply of nominal voltage $+V_S$ [filtered DC supply 22 as shown in Figure 2 and discussed on page 11, lines 28-30 and elsewhere in the specification],

an output connected to said inductor [10], said output having opposed ends [as shown in Figure 1 and discussed on page 11, lines 30-31 and elsewhere in the specification]; and

first and second bridge arms [shown in Figure 1 and discussed on page 11, lines 25-31 and elsewhere in the specification], said arms having

corresponding first and second switches [transistors 20a and 20b as shown in Figure 1 and discussed on page 12, lines 1-7 and elsewhere in the specification] operable in response to first and second switching signals [switching signals 24a and 24b as shown in Figure 2 and discussed on page 12, lines 1-7 and elsewhere in the specification] to be switched between on and off states, wherein switching between various combinations of on and off states [shown in Figures 5a to 5D and discussed on page 20, line 1 through page 22, line 14 and elsewhere in the specification] produces an electrical signal at the opposed ends of said output with voltage pulses at levels of nominally $+V_S$, 0V, and $-V_S$ [as discussed in general on page 12, lines 8-29, discussed in specific on page 20, line 1 through page 22, line 14 and elsewhere in the specification];

a voltage sensor [voltage sensor system 34 shown in Figure 2 and discussed on page 13, lines 12-27 and elsewhere in the specification] for producing a signal indicative of said DC supply voltage [voltage sensor signal 30 shown in Figure 2 and discussed on page 13, lines 18-20 and elsewhere in the specification]; and

a switching signal generator [switching signals generator system 28 shown in Figure 2 and discussed on page 13, lines 4-27 and elsewhere in the specification], responsive to said DC supply voltage signal [22] and said voltage demand signal [12], for generating said first and second switching signals [24a and 24b]."

"13. A method of pulse width modulation control of a bridge circuit [half-bridge circuit 14 as shown generally in Figure 1 and discussed on page 11, lines 10-24 and elsewhere in the specification] comprising an input [filtered DC supply 22 as shown in Figure 2 and discussed on page 11, lines 28-30 and elsewhere in the specification] that receives a DC supply of nominal voltage $+V_S$ [DC supply 36 as shown in Figure 2 and discussed on page 13, lines 12-27 and elsewhere in the specification], an output having an electromagnet connected thereacross [electromagnet 10 as shown generally in Figure 2 and discussed on page 11, lines 10-24 and elsewhere in the specification], and having first and second switches [transistors 20a and 20b as shown in Figure 1 and discussed on page 12, lines 1-7 and elsewhere in the specification], respectively, wherein first and second arms [shown in Figure 1 and discussed on page 11, lines 25-31 and elsewhere in the specification] of said bridge circuit are connected to opposing ends of the electromagnet [10], the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the electromagnet in a pulse width modulation period [voltage demand signal 12 shown in Figure 2 and discussed on page 11, lines 10-24 and elsewhere in the specification];

(b) generating first and second switching signals [switching signals 24a and 24b as shown in Figure 2 and discussed on page 12, lines 1-7 and elsewhere in the the

specification] with reference to the voltage demand signal and with reference to an indication of the DC supply voltage; and

(c) applying the first and second switching signals [24a and 24b] to the first and second switches [20a and 20b], respectively, during said period;

wherein the switching signals [24a and 24b] cause the switches [20a and 20b] to switch between on and off states, switching between various combinations of on and off states [shown in Figures 5a to 5d and discussed on page 20, line 1 through page 22, line 14 and elsewhere in the specification] of the first and second switches producing within the period an electrical signal across the electromagnet [10] with voltage pulses at levels selected from any of $+V_S$, 0V and $-V_S$ [discussed generally on page 12, line 8 to page 13, line 3 and elsewhere in the specification], the first and second switching signals being generated such that an average voltage of the electrical signal supplied to the electromagnet during the period is substantially equal to the desired voltage [discussed generally on page 14, lines 1-11 and elsewhere in the specification]."

"27. A method of operating a switching circuit comprising an input [filtered DC supply 22 as shown in Figure 2 and discussed on page 11, lines 28-30 and elsewhere in the specification] that receives a DC supply of nominal voltage $+V_S$ [DC supply 36 as shown in Figure 2 and discussed on page 13, lines 12-27 and elsewhere in the specification], an output [as shown in Figure 1 and discussed

on page 11, lines 30-31 and elsewhere in the specification] and first and second switches [transistors 20a and 20b as shown in Figure 1 and discussed on page 12, lines 1-7 and elsewhere in the specification], the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output in a period [voltage demand signal 12 shown in Figure 2 and discussed on page 11, lines 10-24 and elsewhere in the specification];

(b) generating first and second switching signals [switching signals 24a and 24b as shown in Figure 2 and discussed on page 12, lines 1-7 and elsewhere in the specification] with reference to the voltage demand signal and with reference to an indication of the DC supply voltage; and

(c) applying the first and second switching signals [24a and 24b] to the first and second switches [20a and 20b] respectively during the period;

wherein the switching signals [24a and 24b] cause the switches [20a and 20b] to switch between on and off states [shown in Figures 5a to 5d and discussed on page 20, line 1 through page 22, line 14 and elsewhere in the specification], switching between various combinations of on and off states of the first and second switches producing an electrical signal at the output with voltage pulses at levels of nominally $+V_S$, 0V and $-V_S$ [discussed generally on page 12, line 8 to page 13, line 3 and elsewhere in the specification], the first and second switching signals being generated such that an average voltage of the electrical signal

supplied to the output during the period is substantially equal to the desired voltage [discussed generally on page 14, lines 1-11 and elsewhere in the specification], wherein the step of generating first and second switching signals comprises generating pulsed first and second switching signals [disclosed in Figures 5a to 5d and discussed on page 20, line 1 to page 22, line 14 and elsewhere], generating said pulsed first and second switching signals according to a rule [as shown in Figure 3a and discussed on page 17, lines 26-29 and elsewhere in the specification] that the signals are to have no more than one pulse per period and generating the first and second switching signals according to the rule [discussed on page 25, line 11 to page 26, line 2 and elsewhere in the specification] that where pulses cannot be centred symmetrically, the longer and shorter sides of the asymmetric pulses are alternated between the leading edge side and the trailing edge side for successive pulses."

"40. A pulse width modulation controller [switching signals generator 28 and half-bridge circuit 14 as shown in Figure 2 and discussed on page 13, lines 4-27 and elsewhere in the specification] for an electromagnet [electromagnet 10 as shown generally in Figure 2 and discussed on page 11, lines 10-24 and elsewhere in the specification] comprising:

a supply input [filtered DC supply 22 as shown in Figure 2 and discussed on page 11, lines 28-30 and elsewhere in the specification] for providing a DC

supply of nominal voltage V_S [DC supply 36 as shown in Figure 2 and discussed on page 13, lines 12-27 and elsewhere in the specification];

a bridge circuit [half-bridge circuit 14 as shown generally in Figure 1 and discussed on page 11, lines 10-24 and elsewhere in the specification] comprising first and second arms [shown in Figure 1 and discussed on page 11, lines 25-31 and elsewhere in the specification] having first and second switches [transistors 20a and 20b as shown in Figure 1 and discussed on page 12, lines 1-7 and elsewhere in the specification] respectively, the first and second arms being connected to opposed ends of the electromagnet [10];

a voltage demand signal indicative of a desired voltage to be supplied to the electromagnet in a pulse width modulation period [voltage demand signal 12 shown in Figure 2 and discussed on page 11, lines 10-24 and elsewhere in the specification];

a switching signal generator [switching signals generator system 28 shown in Figure 2 and discussed on page 13, lines 4-27 and elsewhere in the specification] configured to generate first and second switching signals [switching signals 24a and 24b as shown in Figure 2 and discussed on page 12, lines 1-7 and elsewhere in the specification] with reference to the voltage demand signal [12] and to apply the first and second switching signals [24a and 24b] to the first and second switches [20a and 20b], respectively, during said pulse width modulation period;

wherein said first and second switching signals [24a and 24b] cause the switches [201 and 20b] to switch between on and off states and producing within the pulse width modulation period an electrical signal across the electromagnet [10] with voltage pulses at levels selected from any of V_S, 0V and $-V_S$ [discussed generally on page 14, lines 1-11 and elsewhere in the specification]."

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 6 and 9-11 stand rejected under 35 USC §103 as unpatentable over Dyer (U.S. Patent 4,585,986) in view of Wilcox (U.S. Patent 5,847,554).

Claims 1, 6 and 9-11 stand rejected under 35 USC §103 as unpatentable over Dyer in view of Kern (U.S. Patent 6,081,104).

Claims 13-20 and 23-34 stand rejected on the ground of nonstatutory obviousness-type patenting as being unpatentable over claims 1-28 in U.S. Patent 7,187,567.

VII. ARGUMENT

Appellant's arguments include the fact that the burden is on the Examiner to first and foremost properly construe the language of the claims to determine what structure and/or method steps are covered by that claim. After proper construction of the claim language, the burden is also on the Examiner to

demonstrate where a single reference (in the case of anticipation) or a plurality of references (in the case of an obviousness rejection) teaches each of the structures and/or method steps recited in independent claims 1, 13, 27 and 40.

Furthermore, the Court of Appeals for the Federal Circuit has stated in the case of *In re Rouffet*, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998)

> to prevent the use of hindsight based on the invention to defeat patentability of the invention, this court **requires** the examiner to show a **motivation** to combine the references that create the case of obviousness. In other words, the Examiner **must show reasons** that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. (Emphasis added).

In its recent decision, the U.S. Supreme Court in *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (April 2007), held that it is often necessary for a court to look to interrelated teachings of multiple patents, the effects of demands known to the design community or present in the marketplace and the background knowledge possessed by a person of ordinary skill in the art in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. The Supreme Court held that "[t]o facilitate review [of the Examiner's rational for combining references], this analysis should be made explicit." *Id.* at 1396.

The Supreme Court went on to say that it followed the Court of Appeals for the Federal Circuit's advice that "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (emphasis added, the Supreme Court quoting from the Court of Appeals for the Federal Circuit in *In re Kahn*, 78 USPQ2d 1329 (Fed. Cir. 2006)).

A. The Examiner now finally admits that the Dyer reference contains no disclosure of the claimed "voltage sensor" in independent apparatus claim 1

Appellant's independent claim 1 requires a "voltage sensor for producing a signal indicative of said DC supply voltage."

On page 3, first full paragraph of the Final Rejection, the Examiner admits that "Dyer, however, does not disclose expressly a voltage sensor for producing a signal indicative of said DC supply voltage . . . ." This belated admission is very much appreciated and is dispositive of this issue.

B. The Examiner now finally admits that the Dyer reference contains no disclosure of the claimed "switching signal generator" in independent apparatus claim 1

Appellant's independent claim 1 requires a "switching signal generator . . . ." On page 3, first full paragraph of the Final Rejection, the Examiner admits that

"Dyer, however, does not disclose expressly . . . a switching signal generator, responsive to said DC supply voltage signal and said voltage demand signal, for generating said first and second switching signals."

This belated admission is also very much appreciated and is dispositive of this issue.

C. The Examiner fails to demonstrate where the claimed "voltage sensor" of claim 1 is disclosed in Wilcox and/or Kern

1. Wilcox does not teach the claimed "voltage sensor"

The Examiner, on page 3, second full paragraph, alleges that "Wilcox discloses voltage sensing circuit 320 for sensing the voltage drop of the transistor, which is an indication of the current provided by the regulator and the DC input Vin, see abstract."

Firstly it is noted that the Examiner does not provide any antecedent basis for "the transistor" and Appellant notes that there are numerous transistors illustrated in the various Wilcox figures. Even if the Examiner is referring to the transistors of Figure 3, it is unclear which transistors the Examiner references. Further, because the Examiner indicates "the transistor" he is presumably referencing only a single transistor and there is no single transistor in the Wilcox reference across which the voltage Vin is measured.

If the Examiner is referencing one of transistors 342 and 344, it is noted that Wilcox specifically teaches that these transistors (MOSFET 342 and MOSFET 344) are "driven out of phase with respect to each other to supply current at a regulated voltage to a load" (column 5, lines 23-25). Wilcox at column 4, lines 57-62 specifies that the "voltage drops across both the regulators main and synchronous switching elements as each in turn conducts" is sensed by the sensing circuitry. These transistors, when they are conducting, provide a voltage drop indicative of the current flow therethrough and thus Wilcox is sensing "inductor current" as clearly set out at column 4, lines 60-62. While the supply voltage Vin in Wilcox will affect the current flow through transistors 342 and 344 (when they conduct), the voltage drop across the transistor does not indicate the DC supply voltage Vin.

Moreover, it is significant that Wilcox's voltage drop across the transistors is not sensed simultaneously, in other words, the voltage drop is across only one transistor at a time. See the disclosure in column 4, lines 57-67, as well as that disclosed in column 5, lines 61-67. Wilcox specifically states that "the drain-to-source voltages only provide valid current information while the MOSFETs are ON."

Wilcox states that "during conduction of MOSFET 342, **no valid information** about the I_L [inductor current] is provided by $V_{DS(344)}$[the drain-to-source voltage], because MOSFET 344 is OFF" (col. 5, lines 63-65). Similarly,

Wilcox clearly indicates that "during conduction of MOSFET 344, there is no valid information about I_L [inductor current] provided by $V_{DS(342)}$ [the drain-to-source voltage drop] because MOSFET 342 is OFF" (col. 5, lines 65-67).

The only possible operation which could provide an output indicative of the input supply voltage in Wilcox's Figure 3, is if both MOSFETs 342 and 344 did not conduct and the two outputs provided to the positive inputs to the amplifiers 322 and 324 would indicate V_{IN}. However, Wilcox specifically teaches that "in the time interval between the conduction of MOSFETs 342 and 344, neither the $_{DS}$ measurement provides valid information about I_L, because both switches are off. Importantly, "[d]uring that time interval, blanking circuitry 326 (included as part of sensing circuitry 320) provides blanking signals to sense amplifiers 322 and 324 to disable their outputs" (col. 6, lines 3-6).

In other words, in the only possible circumstance where the Wilcox transistors could provide an indication of the input voltage V_{IN} is when both transistors are not conducting (so as to indicate the voltage drop between V_{IN} and ground) and in that specific instance the blanking circuitry provides blanking signals to the two sense amplifiers 322 and 324 so their outputs are disabled. As a result, the teaching in Wilcox precludes any possibility of measuring V_{IN} and thus teaches away from any sensing of input supply voltage.

In view of the above, it is clear that Wilcox contains no disclosure of the claimed "voltage sensor" or the language relating to "an indication of the DC

supply voltage" and therefore, the Examiner fails to meet his burden of demonstrating how or where the prior art teaches Applicants claimed voltage sensor.

2. Kern does not teach the claimed "voltage sensor"

Turning to the Kern reference and the Examiner's contention on page 5 of the Final Rejection that it discloses the "voltage sensor" of claim 1, the Examiner continues to ignore the major differences between the Dyer and Kern references (previously noted in the November 18, 2008 amendment pages 18-20). While Kern does disclose a DC input voltage sensor, he does not the claimed "voltage sensor" especially one that provides an output "indicative" of the supply voltage.

The Kern patent is directed to a DC-DC power converter for charging a battery and/or for feeding an inverter capable of providing an AC output. In Kern, the only reason for having a voltage sensor is to determine whether or not any power is available, e.g., in the case of a solar cell, to indicate whether or not it is daytime and whether the cell is capable of providing power, and whether the voltage available from the power source is sufficient for charging the battery. It is believed that the Kern sensor merely indicates the operation of the solar cells, but not the voltage – it is much like an on/off flag for the remainder of the power circuit.

Kern does not appear to provide any indication of sensor which provides "a signal indicative of said DC supply voltage." More importantly, there is no disclosure in Kern of the claimed interrelationship of the voltage sensor and the other components, e.g., the "switching signal generator, responsive to said DC supply voltage signal . . . ."

In view of the above, it is clear that Kern contains no disclosure of the claimed "voltage sensor" or the language relating to "an indication of the DC supply voltage" and therefore, the Examiner fails to meet his burden of demonstrating how or where the prior art teaches Applicants claimed voltage sensor.

D. The Examiner fails to demonstrate where the claimed "switching signal generator" of claim 1 is disclosed in Wilcox and Kern

1. Wilcox does not teach the claimed "switching signal generator"

On page 3 of the Final Rejection, after admitting that Dyer is missing any teaching the "switching signal generator," the Examiner fails to identify any aspect of the Wilcox reference that shows the missing structure. The Examiner does allege that Figure 3 of Wilcox "shows oscillator 104, latch 106, drivers 108 and 112, and sensing circuit 320 to control the switching signals provided to switches 342 and 344" but does not suggest that this is a "switching signal generator."

The claim 1 "switching signal generator" is "responsive to said DC supply voltage signal and said voltage demand signal, for generating said first and second switching signals." As noted previously, Wilcox cannot provide any voltage sensing and therefore, there can be no suggestion in Wilcox that any combination of elements (that the Examiner might allege in the future is a "switching signal generator") is responsive to "said DC supply voltage." As noted above, because of the blanking signals provided to the sense amplifiers 322 and 324, such an interrelationship is clearly precluded.

As a result of the above, the Wilcox reference doesn't teach the claimed "switching signal generator" of Appellant's claim 1.

2. Kern does not teach the claimed "switching signal generator"

On page 5 of the Official Action, the Examiner alleges that "controller 82 in turn produces a signal to control the switches of the power converter." Appellant presumes that the Examiner believes this controller is the claimed "switching signal generator" recited in the claims. However, Kerns specifically states that "the voltage sensor 58 allows the controller 82 to sense voltage from the power source 52 to determine when the system 50 is operating during daylight or at night." (col. 6, lines 58-61). Kerns goes on to state that the controller 82 provides signals for turning on and off "the transistor or power switch 128" (col. 7, lines 9-16). However, there is no indication that the signals from controller 82 are supplied to the "first and second bridge arms" as required by Appellants claims.

Where is such an interrelationship disclosed or suggested in the Kerns patent? The claims positively require very specific "first and second switching signals" to which the first and second bridge arms are responsive so as to generate "at the opposed ends of said output with voltage pulses at levels of nominally $+V_S$, 0V, and $-V_S$." There is no allegation by the Examiner that the controller 82 supplies any switching signals to a bridge circuit or that the signals cause the bridge circuit to operate as claimed.

The burden is on the Examiner to identify where the claimed structures and structural interrelationships are shown in the Kern reference and he has failed to meet that burden.

E. The Examiner fails to establish a prima facie case of obviousness of claims 1, 6, and 9-11 under 35 USC §103 over the Dyer/Wilcox combination

In order to shift the burden to the Appellant, the Examiner is required to set out evidence that establishes a prima facie case of obviousness. To meet his or her burden the Examiner must do two things. First, as noted by the Court of Appeals for the Federal Circuit, "the PTO has the burden under §103 to establish a *prima facie* case of obviousness." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "It can satisfy this burden only by showing some objective teaching in the prior art . . . ." Thus all elements set out in the claim must be disclosed somewhere in the prior art combination.

Additionally, even if all claim elements are disclosed in the combination of references, there must be some reason or rational expressed by the Examiner as to how and why one of ordinary skill would pick and chose the claimed elements from the combination of references and then combine them in the claimed manner. This is the required explicit "analysis" as noted by the Supreme Court in the KSR decision discussed above. Additionally, even if a prima facie case of obviousness is made out by the Examiner, it is legally rebutted if Appellant can demonstrate where the cited prior art teaches away from the claimed combination.

As will be seen, with respect to Dyer/Wilcox combination, the Examiner has failed on both accounts to establish a *prima facie* case of obviousness and the evidence of record shows that the prior art would lead one of ordinary skill in the art away from the claimed invention.

1. The Examiner fails to establish that all claimed elements are disclosed in the Dyer/Wilcox combination of references

As noted in Section A above, the Examiner admits that Dyer fails to teach the claimed "voltage sensor." As set out in detail in Section C above, Appellant has demonstrated that Wilcox fails to teach the claimed "voltage sensor." Accordingly, because neither Dyer nor Wilcox teaches this claimed structure, the Patent Office has failed the to meet its burden of identifying sufficient evidence to establish a *prima facie* case of obviousness with respect to the obviousness rejection of claim 1 (and claims 6 and 9-11 dependent thereon) under §103.

Additionally, as discussed in section B above, the Examiner admits that Dyer fails to teach the claimed "switching signal generator." As set out in detail in Section D above, Appellant has demonstrated that Wilcox fails to teach the claimed "switching signal generator." Accordingly, because neither Dyer nor Wilcox teaches this claimed structure, the Patent Office has failed the to meet its burden of identifying sufficient evidence to establish a *prima facie* case of obviousness with respect to the obviousness rejection of claim 1 (and claims 6 and 9-11 dependent thereon) under §103.

Because the Examiner has failed to identify where the Dyer/Wilcox combination discloses at least two of the elements in claim 1, there can be no *prima facie* case of obviousness, and thus any burden of rebutting a *prima facie* case obviousness does not shift to Appellant and instead still rests with the Examiner.

2. The Examiner fails to provide any reasonably explicit "analysis" of his rationale for picking and choosing elements and then combining them in the manner of Claim 1

The above interpretation of the KSR decision was confirmed in a Memorandum from Deputy Commissioner for Patent Operations Margaret A. Focarino on May 3, 2007, in which she said "in formulating a rejection under 35 USC §103(a) based upon a combination of prior art elements, it remains necessary [for the examiner] to identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed."

In the obviousness rejection of claim 1 over Dyer/Wilcox, the Examiner merely concludes that it would be obvious to combine elements from the prior art references, but provides no "reason" or "motivation" for doing so. The statement on page 3 of the Final Rejection ("that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of dyer with the voltage sensor disclosed by Wilcox, col. 5, lines 1-42") contains no "reason," "motivation," or "analysis" for picking and choosing elements and then combining them in the manner of claim 1.

The Examiner only provides a conclusory statement as a reason for combining these two references, i.e., that it would be obvious to one of ordinary skill in the art "to have modified the invention disclosed by Dyer to include the voltage sensor 58 to supply a signal indicative of the DC supply, for the purpose of obtaining a desired output based on the available supply (col. 7 lines 42-47)" (Final Rejection, page 5).

However, even the conclusory statement is incorrect as the Examiner apparently forgets that the Dyer circuit is driven by a relatively stable power source, i.e., battery 7, and one of ordinary skill in the art would not consider it necessary to add the complication of input voltage sensing to Dyer. There would simply be no apparent advantage in sensing the power supply voltage because Dyer obtains all the necessary control information from co-axial shunt 27. Thus,

while it is possible that input voltage sensing could have been added to Dyer, there is no reason for one to do so, especially in the manner expressed by the Examiner on page 5 of the Final Rejection.

Also, while the Examiner cites "column 7, lines 42-47" in his purported rationale for combining references on page 5 (this was questioned in response to the previous official action on page 19 of the November 18, 2008 amendment but has never been clarified or responded to by the Examiner), it is unclear as to whether this is a reference to the Kern patent or the Dyer patent.

Applicant presumes that, although the paragraph discusses Dyer, the citation is, in fact, a reference to the Kern patent, which at column 7, lines 42-48, discusses monitoring "the output voltage from the power source 52" and then controlling the DC-to-DC converter 64 "such that a desired current output signal $C_{DC/DC}$ on the nodes 68, 70 is created." If in fact the Examiner is referencing the Kern reference, this is output voltage monitoring to create a desired **current** output signal. This has nothing to do with a pulse width modulation switching circuit for controlling current to an inductor as required in independent claims 1 and 13.

Again, the Examiner has failed to properly indicate any explicit "analysis" with respect to combining elements taken from the Dyer and Kern references.

Accordingly, the Examiner fails the second test of whether he has made out a *prima facie* case of obviousness.

3. The Dyer and Wilcox references would lead one of ordinary skill in the art away from the claimed invention and thereby rebut any *prima facie* case of obviousness

As noted above in Section D, the primary reference to Dyer teaches that the co-axial shunt 27 is for developing "a voltage signal proportional to the load current." Because the load current feeding an inductor does not reflect the DC supply voltage, the Dyer reference clearly teaches away from any supply voltage sensing.

As also noted in Section D above, in Wilcox, the only time that V_{IN} is available would be when both MOSFETs 342 and 344 are non-conducting (and V_{IN} would be available at the + inputs to sense amplifiers 322 and 324 since one is connected to V_{IN} and the other is connected to ground). Wilcox specifically requires that a blanking signal is applied to the sensing amplifiers 322 and 324 "to disable their outputs." (Wilcox, column 6, lines 2-6). Accordingly, Wilcox specifically teaches a system which would preclude any measurement of V_{IN} and thus teaches away from the claimed invention.

As a result, the adverse teaching in both Dyer and Wilcox would lead one of ordinary skill away from the claimed invention and rebuts any *prima facie* case

of obviousness (even if one had been made and, as noted above, it was not made in view of the evidence of record).

For all of the above reasons, there is no *prima facie* case of obviousness of claim 1 under 35 USC §103 in view of the Dyer/Wilcox combination and, even if there were, any *prima facie* case is specifically rebutted by the adverse teaching in both Dyer and Wilcox.

F. The Examiner fails to establish a prima facie case of obviousness of claims 1, 6, and 9-11 under 35 USC §103 over the Dyer/Kern combination

For the reasons noted above and in Section E, the Examiner is required to set out evidence that establishes a *prima facie* case of obviousness, i.e., all elements set out in the claim must be disclosed somewhere in the prior art combination. In addition, in order to evidence a *prima facie* case of obviousness, there must be some explicit "analysis" by the Examiner as to why the elements would be combined. Further, a *prima facie* case of obviousness is legally rebutted if Appellant can demonstrate where the cited prior art teaches away from the claimed combination.

As will be seen, with respect to Dyer/Kern combination, the Examiner has failed on both accounts to establish a *prima facie* case of obviousness and the evidence of record shows that the prior art would actually lead one of ordinary skill in the art away from the claimed invention.

1. The Examiner fails to establish that all claimed elements are disclosed in the Dyer/Kern combination of references

As noted in Section A above, the Examiner admits that Dyer fails to teach the claimed voltage sensor. As noted in Section C above, Kern fails to teach the specifically claimed voltage sensor and its claimed interrelationship of providing a signal indicative of the DC supply voltage to a switching generator.

As noted in Section B above, the Examiner admits that Dyer fails to teach the claimed "switching signal generator." As set out in detail in Section D above, Appellant has failed to demonstrate that Kern teaches the claimed "switching signal generator."

Accordingly, because neither Dyer nor Kern teach these claimed structures, the Patent Office has failed the to meet its burden of identifying sufficient evidence to establish a *prima facie* case of obviousness with respect to the obviousness rejection of claim 1 (and claims 6 and 9-11 dependent thereon) under §103. Because the Examiner has failed to identify where the Dyer/Kern combination discloses at least two of the elements in claim 1, there can be no *prima facie* case of obviousness, and thus the burden of rebutting a *prima facie* case obviousness does not shift to Appellant and instead still rests with the Examiner.

2. The Examiner fails to provide any reasonably explicit "analysis" of his rationale for picking and choosing elements and then combining them in the manner of Claim 1.

In the obviousness rejection of claim 1 over Dyer/Kern, the Examiner merely concludes that it would be obvious to combine elements from the prior art references, but provides no "reason" or "motivation" for doing so.

The statement on page 5 of the Final Rejection is merely conclusory (that "it would have been obvious to one of ordinary skill in the art at the time the invention to have modified the invention disclosed by Dyer to include the voltage sensor 58 to supply a signal indicative of the DC supply, for the purpose of obtaining a desired output based on the available supply (col. 7, lines 42-47)"). However, this statement contains no "reason," "motivation," or "analysis" for picking and choosing elements and then combining them in the manner of claim 1.

Accordingly, the Examiner fails the second test of whether he has made out a *prima facie* case of obviousness in view of the Dyer/Kerns combination.

3. The Dyer reference would lead one of ordinary skill in the art away from the claimed invention and thereby rebut any *prima facie* case of obviousness

As noted above in Section C, the primary reference to Dyer teaches that the co-axial shunt 27 is for developing "a voltage signal proportional to the load current." Because the load current feeding an inductor does not reflect the DC supply voltage, the Dyer reference clearly teaches away from any supply voltage sensing.

As a result, the adverse teaching in Dyer would lead one of ordinary skill away from the claimed invention and rebuts any *prima facie* case of obviousness (even if one had been made and, as noted above, it was not made in view of the evidence of record).

For all of the above reasons, there is no *prima facie* case of obviousness of claim 1 under 35 USC §103 in view of the Dyer/Kern combination and, even if there were, any *prima facie* case is specifically rebutted by the adverse teaching in Dyer.

G. The Examiner fails to establish a *prima facie* case of non-statutory obviousness double patenting of claims 13-20 and 23-34 in view of US Patent 7,187,567

The Examiner admits that independent method claim 13 is not identical to claim 1 in US Patent 7,187,567, but suggests that the claims are not "patentably distinct from each other because." This language is contained in section 7, beginning on page 7 of the Official Action and Applicant wonders whether the Examiner intended to include additional subject matter after the word "because" which is at the end of the sentence.

Applicant also notes that current method claim 13 is a method of "pulse width modulation control of a bridge circuit" whereas claim 1 in the '567 is directed to a method of operating a bridge circuit. Pending claim 13 relates to an "electrical signal to be supplied to the electromagnet in a plus width modulation

period" whereas the '567 patent does not mention pulse width modulation. Also it is noted that in the wherein clause in the '567 patent claim 1, there is no reference to "producing within the period an electrical signal across the electromagnet" whereas this is the language in pending claim 13.

In view of these distinct differences between claim 1 of the '567 patent and pending claim 13 of the appealed from claims, it is submitted that the appealed from claims are patentably distinct from the claims of the '567 patent.

With respect to claim 40, there is a bare allegation by the Examiner that claims 1, 7 and 12 of the '567 patent disclose the limitations of claim 40. However, claim 40 is directed to a pulse width modulation controller for an electromagnet and is not directed to a "method of operating a bridge circuit" specified in the '567 patent. Accordingly, claim 40, to the extent it may be rejected (as noted above, there is no allegation of rejection of claim 40 under obviousness-type double patenting grounds, only claims 13-20 and 23-34), the rejection is respectfully traversed.

The Examiner's indication that independent claims 13, 24 and 40 and claims dependent thereon "would be allowable except for the double patent rejection above" is very much appreciated.

In the event the Board confirms that the pending claims 13-20 and 23-34 (and claim 40, if this is in fact rejected) are properly rejection under non-statutory obviousness-type double patenting grounds over the '567 patent, Applicant may

file a Terminal Disclaimer to remove this impediment to patent issuance with respect to those claims. Applicant will reserve judgment and reserve payment of the Terminal Disclaimer fee pending the decision by the Board in this matter.

VIII. CONCLUSION

In the pending Final Rejection, the Examiner admits that the primary reference to Dyer fails to teach at least two positively recited structures in independent claim 1, i.e., "voltage sensor" and the "switching signal generator." The Examiner has failed to identify any structure in the Wilcox reference which comprises a "voltage sensor" or a "switching signal generator." While Kern discloses a voltage sensor, it does not disclose a voltage sensor and the voltage sensor interrelationships specified in Applicant's independent claim 1 and certainly does not disclose the switching signal generator as claimed. Accordingly, the Patent Office fails to meet the first test of a *prima facie* case of obviousness, i.e., disclosure of all claimed elements and claimed interrelationships.

Secondly, the Examiner fails to provide the required explicit "analysis" of his reasons for picking and choosing elements and combining them in the manner of Applicant's claims and so the Examiner's case fails the second test of a prima facie case of obviousness. Thirdly, even with the above deficiencies, should the Board conclude that the Examiner has established a *prima facie* case of

obviousness, Applicant notes that both the Dyer and Wilcox references contain teachings which preclude the specified combinations, i.e., Dyer with the coaxial shunt 27 for developing a voltage signal "proportional to the load current" and not the input voltage and Wilcox's precluding of any reading of input supply voltage, clearly would lead one of ordinary skill in the art away from the claimed combination.

As a result of the above, there is simply no support for the rejections of Appellant's independent claims or claims dependent thereon under 35 USC §103. Thus, and in view of the above, the rejection of claims 1, 6, 9-11, 13-34 and 38-42 under 35 USC §103 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

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Enclosure

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IX. CLAIMS APPENDIX

1. A pulse width modulation switching circuit, responsive to a voltage demand signal, for controlling current supplied to an inductor from a direct current (DC) supply voltage, said switching circuit comprising:

a bridge circuit, said bridge circuit comprising:

an input operable to receive a direct current, DC, supply of nominal voltage $+V_S$,

an output connected to said inductor, said output having opposed ends; and

first and second bridge arms, said arms having corresponding first and second switches operable in response to first and second switching signals to be switched between on and off states, wherein switching between various combinations of on and off states produces an electrical signal at the opposed ends of said output with voltage pulses at levels of nominally $+V_S$, 0V, and $-V_{S;}$

a voltage sensor for producing a signal indicative of said DC supply voltage; and

a switching signal generator, responsive to said DC supply voltage signal and said voltage demand signal, for generating said first and second switching signals.

6. A switching circuit according to claim 1, further comprising a current sensor for producing a signal indicative of the current flowing through the output.

9. A switching circuit according to claim 1, wherein the bridge circuit is a half-bridge with the third and fourth arms having diodes.

10. A switching circuit according to claim 1, wherein the first and second switches are transistors.

11. A switching circuit according to claim 1, wherein said inductor comprises an electromagnet connected across the output of the bridge circuit.

13. A method of pulse width modulation control of a bridge circuit comprising an input that receives a DC supply of nominal voltage $+V_S$, an output having an electromagnet connected thereacross, and having first and second switches, respectively, wherein first and second arms of said bridge circuit are connected to opposing ends of the electromagnet, the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the electromagnet in a pulse width modulation period;

(b) generating first and second switching signals with reference to the voltage demand signal and with reference to an indication of the DC supply voltage; and

(c) applying the first and second switching signals to the first and second switches, respectively, during said period;

wherein the switching signals cause the switches to switch between on and off states, switching between various combinations of on and off states of the first and second switches producing within the period an electrical signal across the electromagnet with voltage pulses at levels selected from any of $+V_S$, 0V and $-V_S$, the first and second switching signals being generated such that an average voltage of the electrical signal supplied to the electromagnet during the period is substantially equal to the desired voltage.

14. The method of claim 13, wherein at least one of the first and second switching signals is generated with reference to a voltage signal indicative of the DC supply such that the at least one first or second switching signal compensates for fluctuations in the DC supply.

15. The method of claim 14, wherein the voltage signal is passed through a filter to obtain a predictive measure of fluctuations in the DC supply.

16. The method of claim 15, wherein the voltage signal is passed through a finite impulse response filter.

17. The method of claim 13, wherein at least one of the first and second switching signals is generated to compensate for a voltage drop across a diode and/or transistor in the switching circuit.

18. The method of claim 17, wherein the at least one first or second switching signal is generated with reference to a current signal indicative of the current flowing through the output and a representative resistance of the diode or transistor.

19. The method of claim 13, wherein at least one of the first or second switching signals is generated with reference to a measure of a voltage offset caused by a slow response in generating the first or second switching signals.

20. The method of claim 13, wherein the switching circuit comprises a bridge circuit having an input that receives the DC supply, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output.

21. The method of claim 20, wherein the bridge circuit is a half-bridge with the third and fourth arms having diodes.

22. The method of claim 20, wherein the first and second switches are transistors and the method comprises the step of switching the transistors between on and off states corresponding to substantially minimum voltage drop and substantially minimum current flow, respectively, through the transistors.

23. The method of claim 13 comprising the step of generating pulsed first and second switching signals.

24. The method of claim 23 comprising the step of generating the first and second switching signals according to a rule that the first and second switches are not switched concurrently.

25. The method of claim 23 comprising the step of generating the first and second switching signals according to a rule that the signals are to have no more than one pulse per period.

26. The method of claim 25 comprising the step of generating the first and second switching signals according to a rule that any pulse should be positioned symmetrically about the centre of the period.

27. A method of operating a switching circuit comprising an input that receives a DC supply of nominal voltage $+V_S$, an output and first and second switches, the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output in a period;

(b) generating first and second switching signals with reference to the voltage demand signal and with reference to an indication of the DC supply voltage; and

(c) applying the first and second switching signals to the first and second switches respectively during the period;

wherein the switching signals cause the switches to switch between on and off states, switching between various combinations of on and off states of the first and second switches producing an electrical signal at the output with voltage pulses at levels of nominally $+V_S$, 0V and $-V_S$, the first and second switching signals being generated such that an average voltage of the electrical signal supplied to the output during the period is substantially equal to the desired voltage, wherein the step of generating first and second switching signals

comprises generating pulsed first and second switching signals, generating said pulsed first and second switching signals according to a rule that the signals are to have no more than one pulse per period and generating the first and second switching signals according to the rule that where pulses cannot be centred symmetrically, the longer and shorter sides of the asymmetric pulses are alternated between the leading edge side and the trailing edge side for successive pulses.

28. The method of claim 23 comprising the step of generating the first and second switching signals according to a pulse width modulation scheme.

29. The method of claim 23 comprising the step of noise shaping the first and second switching signals.

30. The method of claim 13 comprising the step of receiving a current demand signal indicative of a desired current to be supplied to the output in a period and calculating the voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output that results in the electrical signal being supplied to the output during the period with a current substantially equal to the desired current.

31. The method of claim 30, wherein the step of calculating the voltage demand signal is performed with reference to a model of the load characteristic of a load connected to the output.

32. The method of claim 30 further comprising the step of generating the voltage demand signal with reference to a current signal indicative of the current flowing through the output.

33. A computer program comprising program code means for performing the method steps of claim 13 when the program is run on a computer associated with the switching circuit.

34. A computer program product comprising program code means stored on a computer readable medium for performing the method steps of claim 13 when the program is run on a computer associated with the switching circuit.

38. The method of claim 13, wherein, when the desired voltage is of less than a predetermined magnitude, the first and second switching signals are generated such that the electrical signal comprises voltage pulses of both V_S and $-V_S$ within the period.

39. The method of claim 13, wherein, when the desired voltage is of at least predetermined magnitude, the first and second switching signals are generated such that the electrical signal comprises voltage pulses of either V_S or $-V_S$ within the period.

40. A pulse width modulation controller for an electromagnet comprising:

a supply input for providing a DC supply of nominal voltage V_S;

a bridge circuit comprising first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the electromagnet;

a voltage demand signal indicative of a desired voltage to be supplied to the electromagnet in a pulse width modulation period;

a switching signal generator configured to generate first and second switching signals with reference to the voltage demand signal and to apply the first and second switching signals to the first and second switches, respectively, during said pulse width modulation period;

wherein said first and second switching signals cause the switches to switch between on and off states and producing within the pulse width modulation period an electrical signal across the electromagnet with voltage pulses at levels selected from any of V_S, 0V and $-V_S$.

41. The controller of claim 40 wherein the switching signal generator is configured, when the desired voltage is of less than a predetermined magnitude, to generate the first and second switching signals to provide the electrical signal comprising voltage pulses of both V_S and $-V_S$ within the period.

42. The controller of claim 40 wherein the switching signal generator is configured, when the desired voltage is of at least a predetermined magnitude, to generate the first and second switching signals to provide the electrical signal comprising voltage pulses of either V_S or $-V_S$ within the period.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.